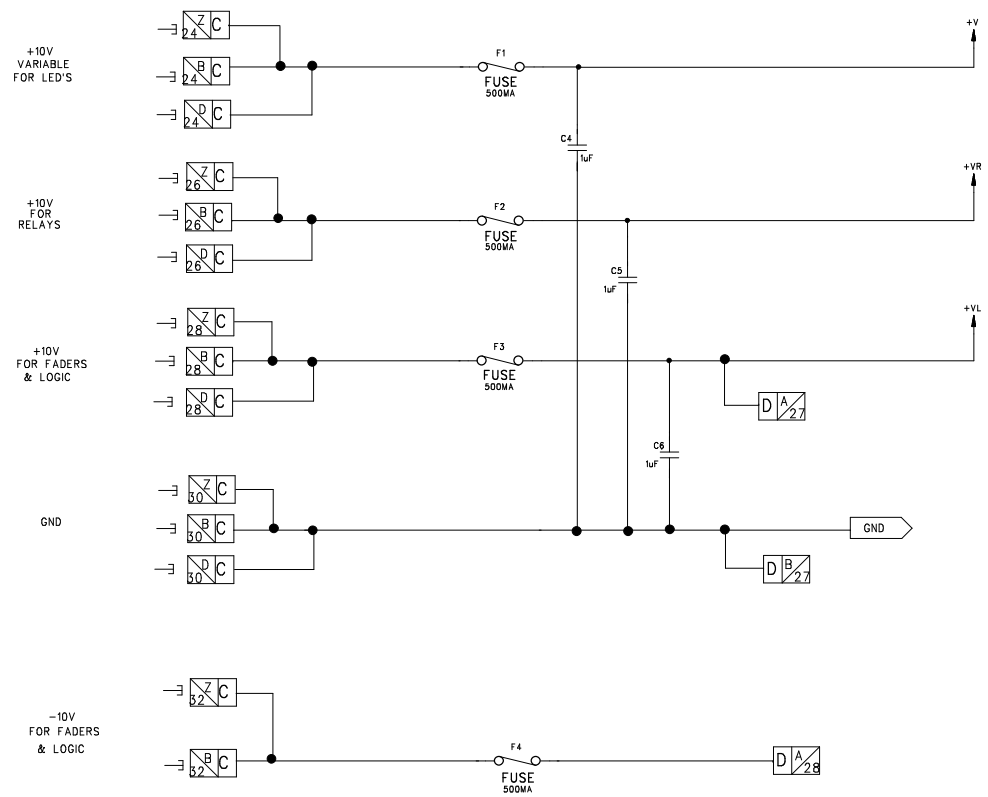
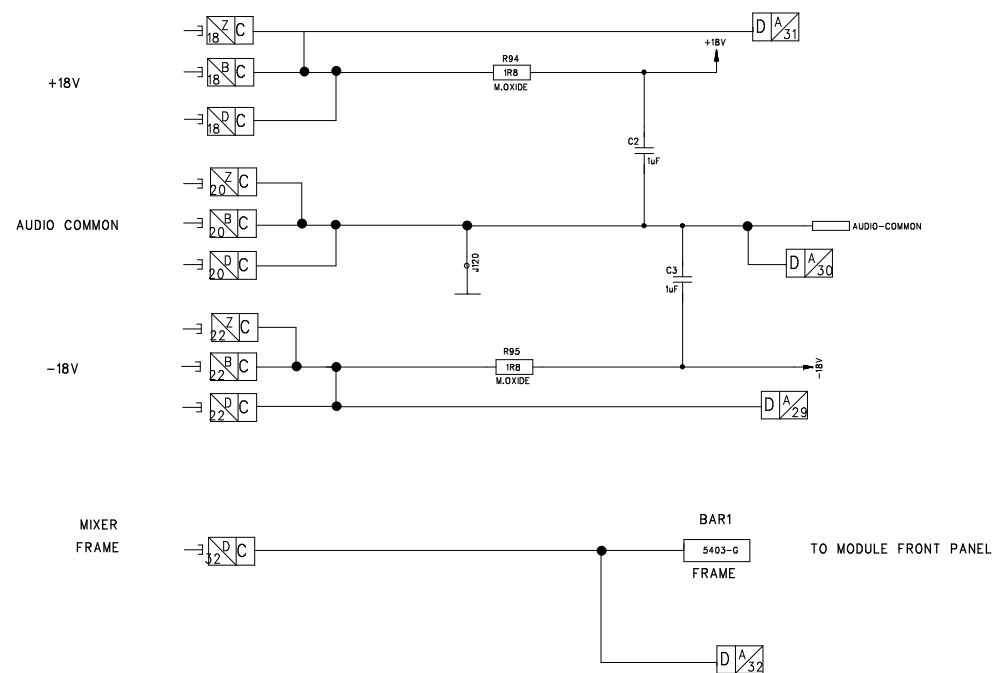
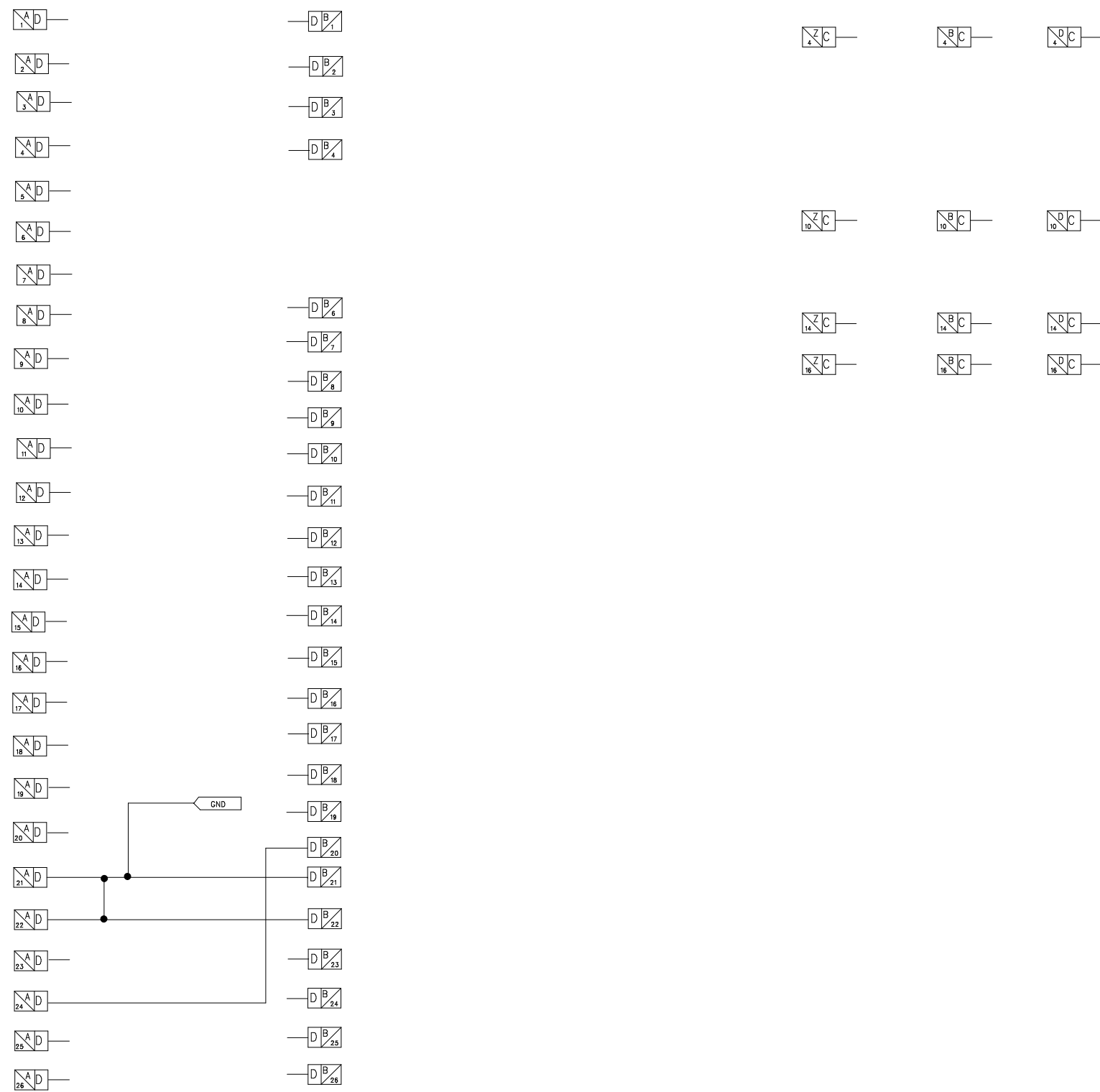


| REDRAWN IN POWER LOGIC | | | | | | | | | |
|---|--|------------------------|----|----------|----------|----------|------|--------------|--|
| TITLE EQUALIZER FOR J-TYPE INPUT CHANNEL | | DESIGNER | TW | 18.11.91 | DATE | 18.11.91 | DATE | | |
| | | DRAWN | TW | 1 | 18.11.91 | TW | 5 | | |
| | | CHECKED | XX | 2 | 26.11.91 | TW | 6 | | |
| | | APPROVED | XX | 3 | 02.12.91 | TW | 7 | | |
| | | 1st ISSUE | 4 | | | | 8 | | |
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REDRAWN IN POWER LOGIC

| TITLE | | | | DESIGNER | | | | DATE | | | |
|--|--|--|--|------------------------|----|---|----------|------|---|--|--------------|
| POWER CONNECTIONS INPUT CHANNEL J-TYPE | | | | DRAWN | TW | 1 | 06.01.92 | TW | 5 | | |
| | | | | CHECKED | XX | 2 | | | 6 | | |
| | | | | APPROVED | XX | 3 | | | 7 | | |
| | | | | 1st ISSUE | | 4 | | | 8 | | |
| | | | | CADAC DRWG No. A1.6980 | | | | | | | SHEET 4 OF 5 |



REDRAWN IN POWER LOGIC

| | | | | | | |
|---|-----------|----|----|----------|----|--------------|
| TITLE UNUSED PINS FOR J-TYPE I/P CHANNEL | DESIGNER | TW | 88 | DATE | 88 | DATE |
| | DRAWN | TW | 1 | 02.12.91 | TW | 5 |
| | CHECKED | XX | 2 | 08.12.92 | TW | 6 |
| | APPROVED | XX | 3 | | | 7 |
| | 1st ISSUE | | 4 | | | 8 |
| CADAC DRWG No. A1.6980 | | | | | | SHEET 5 OF 5 |